RESPONSE UNDER 37 C.F.R. §1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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J.M Culler
7/23/02

Applicant(s): Eduard A. Cartier, et al.

Serial No: 09/413,462

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For: SILICATE GATE DIELECTRIC

Examiner: Lourdes C. Cruz

Art Unit: 2827

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Dated: July 18, 2002

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Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

RESPONSE UNDER 37 C.F.R. §1.116

Sir:

In response to the Office Action dated June 4, 2002, applicants submit the following amendments and remarks for entry of record in the above-identified patent application.

IN THE CLAIMS:

Please amend Claims 21, 28 and 34 to read as follows:

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Dated: July 18, 2002

Tricia Tucci

D1

21. (Thrice Amended) A semiconductor structure comprising at least one metal silicate dielectric material that is in direct contact with a silicon oxide layer, said silicon oxide layer is located directly on a Si-containing substrate, and an electrically conductive contact located directly on an upper horizontal surface of each of said metal silicate dielectric materials.

D2

28. (Twice Amended) A field effect transistor comprising:

a Si-containing semiconductor substrate;

spaced apart source/drain regions in said substrate defining a channel region therein;

a dielectric layer located atop said channel region, said dielectric layer including a bottom SiO_2 layer and a top metal silicate layer; and

a gate electrode located directly on an upper horizontal surface of said top metal silicate layer.

D3

34. (Four Times Amended) A capacitor comprising a metal silicate dielectric material and a SiO_2 layer sandwiched between top and bottom electrode materials, wherein said metal silicate dielectric material is located directly atop said SiO_2 layer and said top electrode is located directly on an upper horizontal surface of said metal silicate dielectric material.

REMARKS

Favorable reconsideration of this application in view of the foregoing amendments and remarks to follow is respectfully requested. Since the present amendment raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claims 21, 28 and 34 in the manner indicated supra. Specifically, applicants have amended Claim 21 to positively recite that an electrically conductive contact

is located directly on an upper horizontal surface of each of the metal silicate dielectric materials present in the claimed structure. Support for this amendment to Claim 21 is found at Page 11, lines 9-15 of the specification of the instant application.

Insofar as Claims 28 and 34 are concerned, applicants have also amended those claims to positively recite that either a gate electrode or a top electrode is located directly on an upper horizontal surface of the metal silicate dielectric material. Support for this amendment to Claims 28 and 34 is found in FIGS 10 and 11 as well as at Page 11, lines 9-15.

Since the above amendments to the claims do not introduce any new matter into the application, entry thereof is respectfully requested. Moreover, applicants submit that the above amendments should also be entered since the amendments clarify and further limit the claimed structures recited therein to ones wherein the electrically conductive contact, e.g., gate electrode or top electrode, is located directly on upper horizontal surface of the claimed metal silicate dielectric material.

As required by 37 C.F.R. §1.121, applicants have attached a marked-up version of the changes made to the claims by the current amendment. The marked-up attachment is captioned "**VERSION WITH MARKINGS SHOWING CHANGES MADE**".

In the present Office Action, the Examiner objects to the disclosure of the present application since the same allegedly does not include a description of FIG 11 which was added in Applicants' Amendment and Response dated March 15, 2002. Specifically, the Examiner avers that the previous submission **only** included a brief description for FIG 10. Applicants respectfully disagree with the Examiner's averment that the previous submission only included a brief description for FIG 10. Instead, at the top of Page 2 of the previous

submission to the USPTO a brief description of FIG 11 was provided. See also the attachment accompanying Applicants' Amendment and Response dated March 15, 2002.

In view of the previous submission and the remarks provided above, applicants respectfully submit that the objection to the disclosure of the present application has been obviated; therefore reconsideration and withdrawal of the instant objection are respectfully requested.

Claims 21-24, 26-31 and 34 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 5,313,089 to Jones, Jr. ("Jones, Jr."). Claim 25 stands rejected under 35 U.S.C. §103 as allegedly unpatentable over Jones, Jr. Claim 33 stands rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of Jones, Jr. and U.S. Patent No. 6,236,094 to Wright ("Wright").

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the applied prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: The absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants submit that Jones, Jr. does not anticipate Claims 21-24 and 26-27 of the present application since the applied reference does not disclose a semiconductor structure comprising an electrically conductive contact that is located directly on an upper surface of each of the metal silicate dielectric materials, as is presently claimed. In contrast, Jones, Jr.

discloses in FIG 5 a capacitor comprising high-permittivity dielectric region 36 which is sandwiched between vertical conductive regions 38' and 38''. The high-permittivity material lies atop isolation or buffer layer 34 which is formed on dielectric material 30. Thus, Jones, Jr. discloses a structure in which the electrical conductive contacts 38' and 38'' are located on **vertical** sidewalls of the high permittivity material. In FIGS 7-9 of Jones, Jr. there is disclosed forming polish stop layer 44 atop the high-permittivity region. The polish stop layer is not an electrical conductive contact material. In FIG 10, Jones, Jr. discloses forming layer 62 atop the surface of high- permittivity material 60. Layer 62 is defined as being an oxide such as TEOS, not an electrically conductive contact.

Insofar as Claims 28-31 and 33 are concerned, applicants respectfully submit that Jones, Jr. does not disclose applicants' claimed FET which includes a Si-containing semiconductor substrate; spaced apart source/drain regions in said substrate defining a channel region therein; a dielectric layer located atop said channel region, said dielectric layer including a bottom SiO_2 layer and a top metal silicate layer; and a gate electrode located directly on upper horizontal surface of the top metal silicate layer. In contrast, the FET disclosed in Jones, Jr. comprises substrate 12, source/drain regions 18 and 16, gate dielectric 24 and gate electrode 26. In accordance with Jones, Jr. (See, Col. 3, lines 36-37) gate dielectric 24 is SiO_2. Applicants find no disclosure in Jones, Jr. of a FET structure which includes a metallic silicate/SiO_2 stack as the gate dielectric material, where a gate electrode is located directly atop an upper horizontal surface of the metal silicate dielectric material.

With regard to Claim 34, applicants respectfully submit that the claimed capacitor structure recited in Claim 34 is not anticipated by the disclosure of Jones, Jr. since the applied reference does not disclose a capacitor comprising a metal silicate dielectric material and a

SiO_2 layer sandwiched between top and bottom electrode materials, wherein said at least one metal silicate is located directly atop said SiO_2 layer and the top electrode is located directly on an upper horizontal surface of the metal silicate. Instead, Jones, Jr. disclose a capacitor structure comprising high-permittivity dielectric region 36 which is sandwiched between vertical conductive regions 38' and 38''. The high-permittivity material lies atop isolation or buffer layer 34 which is formed on dielectric material 30. The prior art capacitor structure has vertical conductive regions, not an electrode that is present on a horizontal surface of a metal silicate, as presently claimed.

Applicants submit that Jones, Jr. teaches away from using planar capacitor devices at Col 1, lines 35-48. In Jones, Jr., the capacitor electrodes are located on the vertical sidewalls of the dielectric material.

The foregoing remarks clearly indicate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by Jones, Jr. Applicants thus respectfully submit that the instant §102(b) rejection has been obviated; therefore the anticipation rejection can and should be withdrawn.

With regard to the §103 rejection to Claim 25 citing Jones, Jr. is concerned, applicants submit that the above remarks hold equally well here for this obviousness rejection; therefore those remarks are incorporated herein by reference. To reiterate: Jones, Jr. does not disclose a structure in which an electrically conductive contact, such as a gate electrode or capacitor electrode, is located directly on an upper horizontal surface of a metal silicate dielectric material. Instead, Jones, Jr. provides structures where the conductive material is located on the vertical sidewalls of the dielectric material.

Applicants further submit that Jones, Jr. teaches away from using planar capacitor devices. See Col 1, lines 35-48. As such, the rejection under 35 U.S.C. §103 to Claim 25 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Insofar as the §103 rejection to Claim 33 is concerned, applicants submit that the applied prior art references of Jones, Jr. and Wright do not teach or suggest applicants' claimed FET structure which includes a Si-containing semiconductor substrate; spaced apart source/drain regions in said substrate defining a channel region therein; a dielectric layer located atop said channel region, said dielectric layer including a bottom SiO_2 layer and a top metal silicate layer; and a gate electrode located directly on an upper horizontal surface of the top silicate layer. The primary reference spurring the §103 rejection, i.e., Jones, Jr., is deficient for the same reasons as mentioned above concerning the §102(b) rejection; therefore those remarks are incorporated herein by reference. To reiterate: the FET disclosed in Jones, Jr. comprises substrate 12, source/drain regions 18 and 16, gate dielectric 24 and gate electrode 26. In accordance with Jones, Jr., (See, Col. 3, lines 36-37) gate dielectric 24 is SiO_2. Applicants find no disclosure in Jones, Jr., of a FET structure which includes a metallic silicate/SiO_2 stack as the gate dielectric material having a gate electrode located directly on the upper horizontal surface of the metallic silicate layer.

The above defect in Jones, Jr. is not alleviated by Wright since the applied reference does not teach or suggest applicants' claimed FET which includes a gate dielectric layer that comprises a bottom SiO_2 layer and a metal silicate formed thereon, wherein a gate electrode is located atop an upper horizontal surface of the metal silicate. In contrast, the FET structure disclosed in Wright comprises substrate 302 having source and drain regions 310 and 312 formed therein which define channel region 305. The prior art FET includes gate dielectric

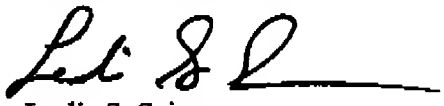
306 such as SiO_2 formed above the channel, gate electrode 308 formed atop of the gate dielectric and low resistance metal such as Al or W formed atop the gate electrode. Applicants respectfully submit the Wright does not teach or suggest the claimed dielectric stack as the gate dielectric for a FET.

The rejection under 35 U.S.C. §103 citing the combination of Jones, Jr. and Wright has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Each of the §103 rejections also fails because there is no motivation in the applied references which suggest modifying the structures disclosed therein to include an electrically conductive contact such as a gate electrode or capacitor electrode located directly on a horizontal surface of a metal silicate dielectric material. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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